ALD ATO nanolaminates with adjustable electrical properties

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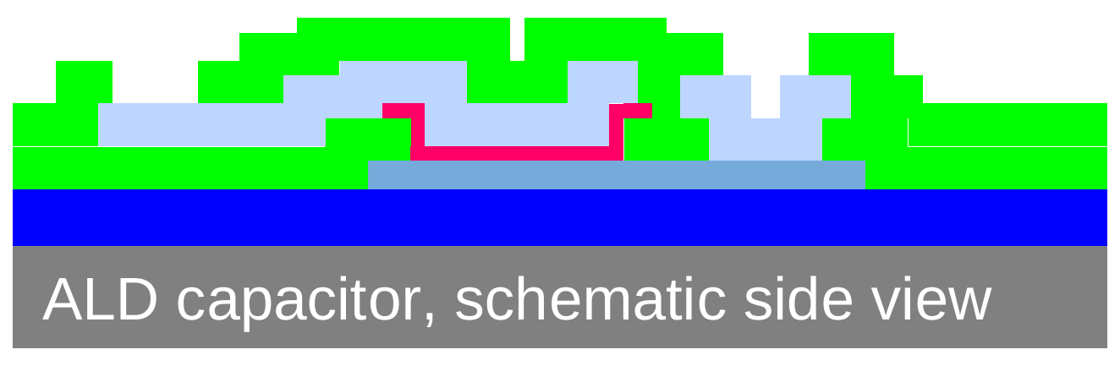
GOAL

- "Multi-purpose" ALD process for MEMS and other applications
- Al_2O_3 and TiO_2 with complementary properties (electrical, optical, etc.) in use at VTT Micronova cleanroom → tune properties using Al_2O_3/TiO_2 layers (i.e., ATO)
- This work: analysis of electrical characteristics of ATO layers

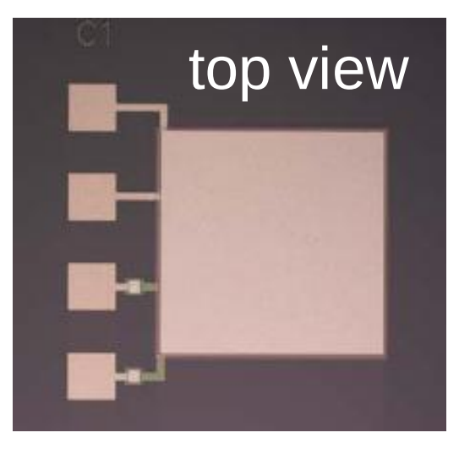
EXPERIMENT



🟦 Mo+Al
🟥 ALD
🟩 PECVD ox or LTO
🟦 Mo
🟦 SiO2
⬛ Si

Capacitors (active area 0.25-4.0 mm^2)

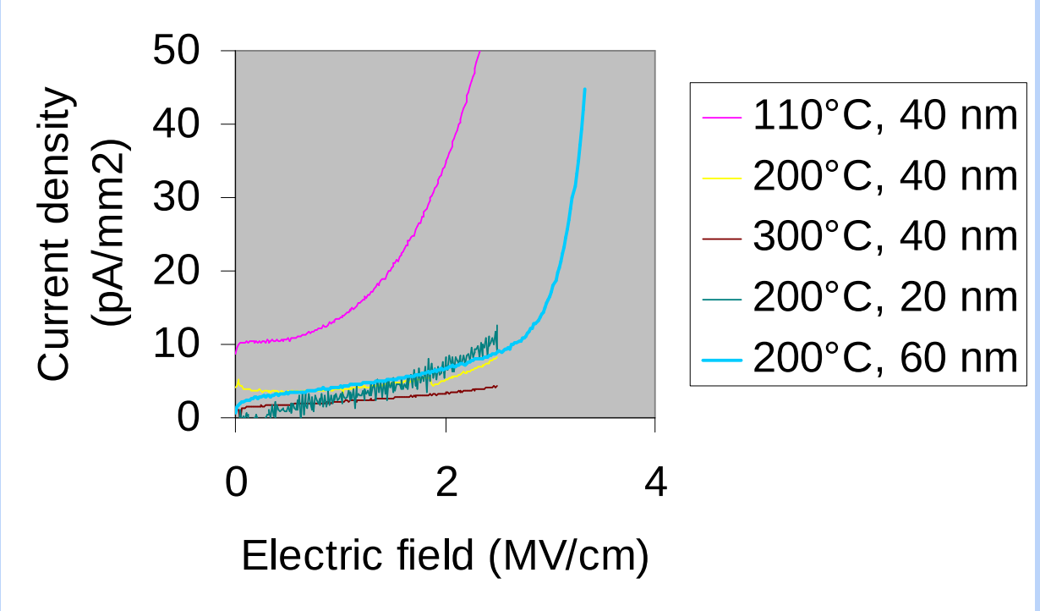
- Substrate: 150 mm Si wafers
- Bottom isolation: 2 µm thermal SiO_2
- Bottom electrode Mo, 250 nm
- Inter-level dielectric: SiO_2 (LTO), 800 nm
- Active dielectric: ALD, ~20-60 nm
- Top electrode: 250 nm Mo + 1 µm Al
- Passivation: SiO_2 (PECVD), 500 nm
- IV,CV: Agilent 4155C and 4294A equipment

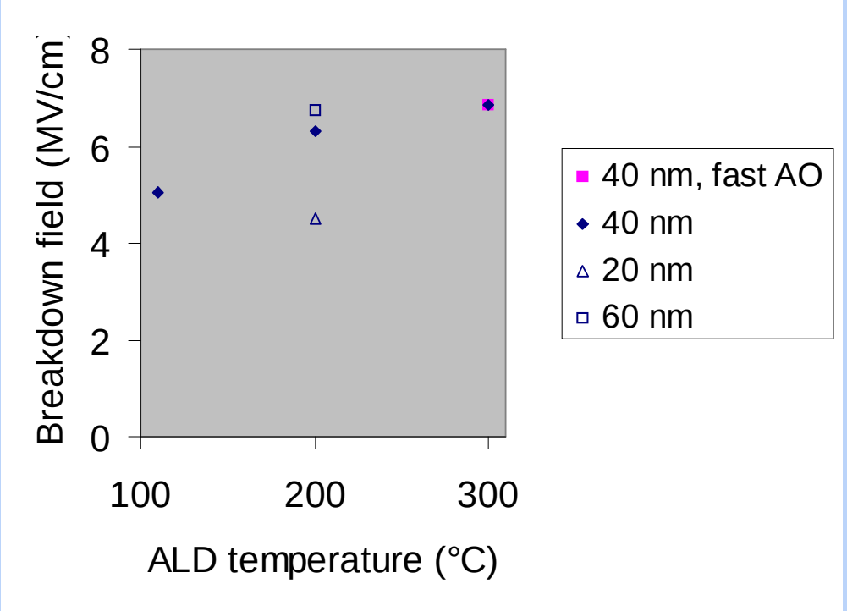


ALD details: Picosun SUNALE^{TM} R-150 ALD reactor, $AlMe_3$/H_2O and $TiCl_4$/H_2O processes. Cycle times 0.1 ($AlMe_3$ or $TiCl_4$), 4 s purge, 0.1 s H_2O, 4 s purge (fast recipe at 300°C: 1 s purges). ATO grown at 200°C, single Al_2O_3 and TiO_2 layers at 110-300°C. In ATO, Al_2O_3 target thickness 1-3 nm; TiO_2 target thickness 3 nm (or 2 nm); Al_2O_3 as starting and ending layer. Number of Al_2O_3/TiO_2 bilayers varied from 6 to 10 to achieve total thickness ~40 nm. After ALD, some samples were heated to 500°C to simulate the effect of possible post-ALD steps in MEMS.

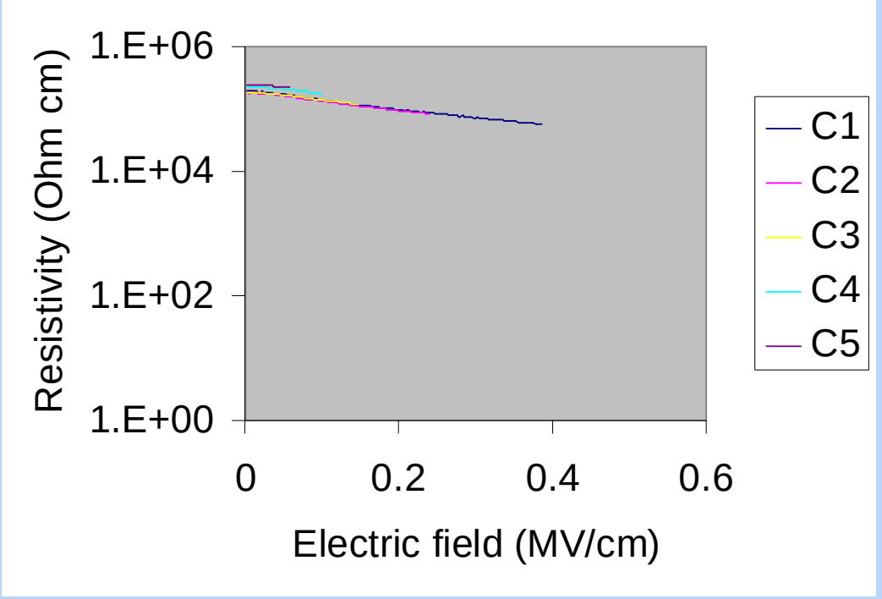
ELECTRICAL CHARACTERISTICS: Al_2O_3 and TiO_2

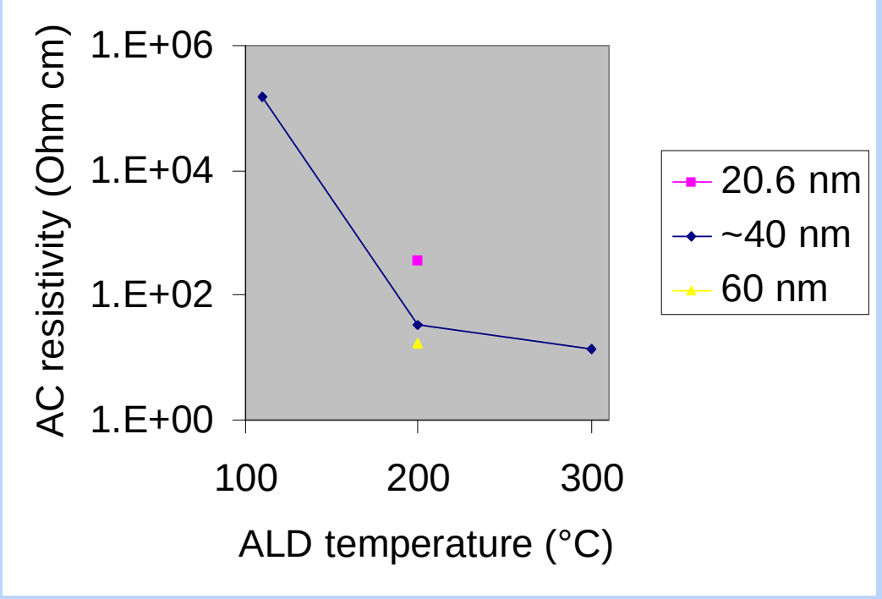
ALD-Al_2O_3 is a high-quality insulator, also in as-deposited state:





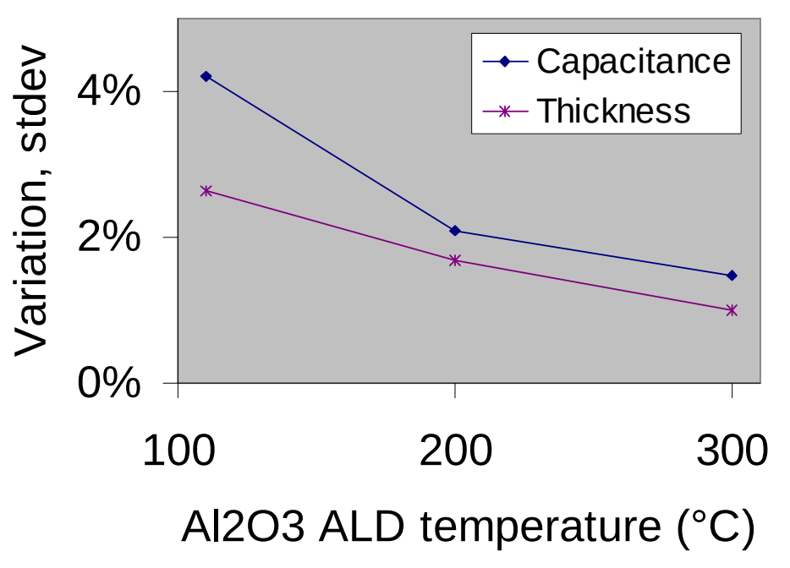
ALD-TiO_2 is semi-insulating. Resistivity is dynamic and a sensitive function of process parameters (temperature, thickness, etc.)

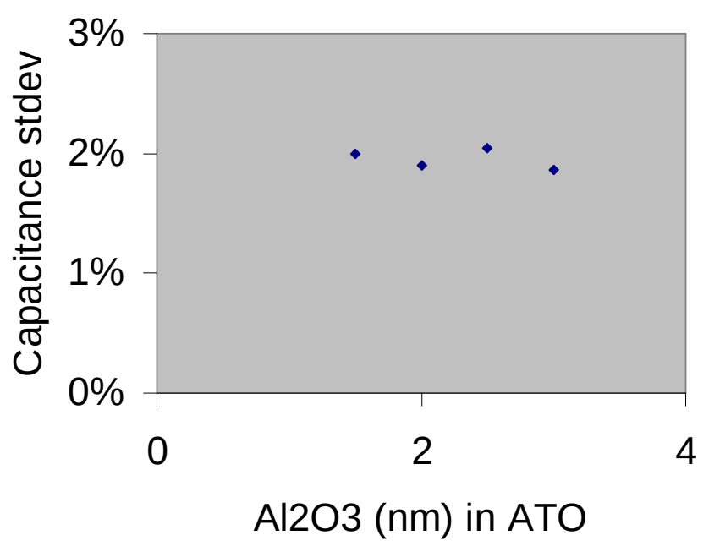


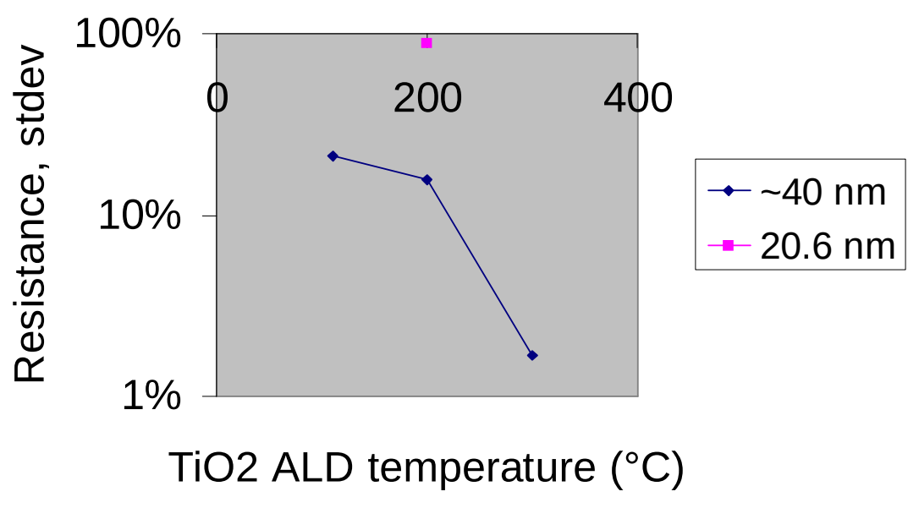


UNIFORMITY ON WAFER

Over 200 capacitors on wafer were measured. Stdev of Al_2O_3 and ATO capacitance in line with stdev of layer thickness (~2% for 200°C deposition), but for TiO_2, stdev of resistivity markedly higher.

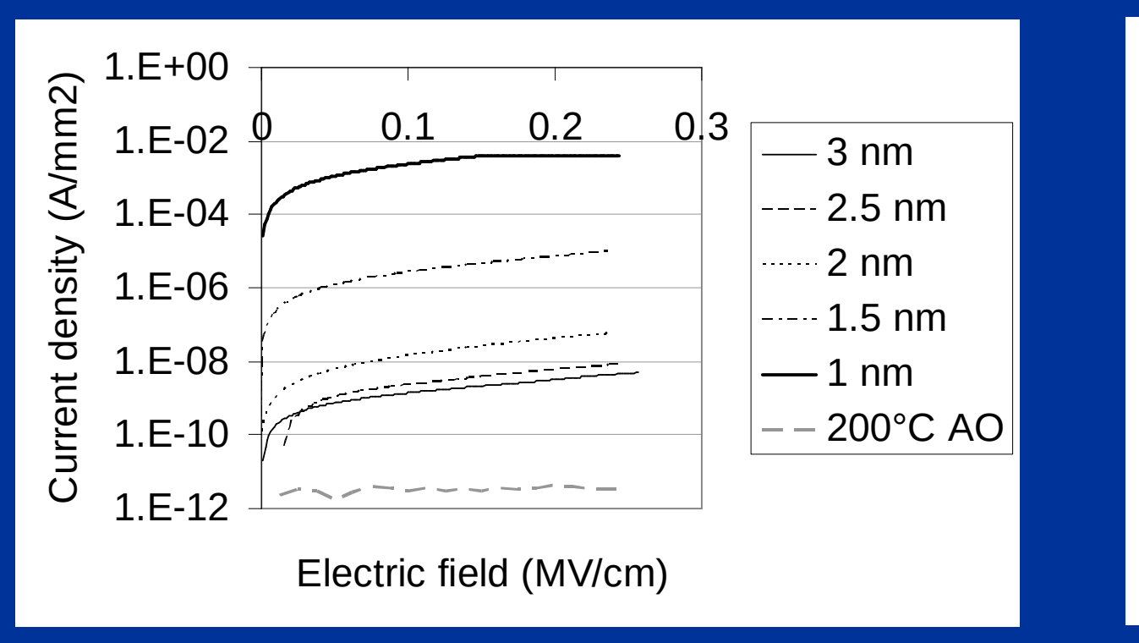


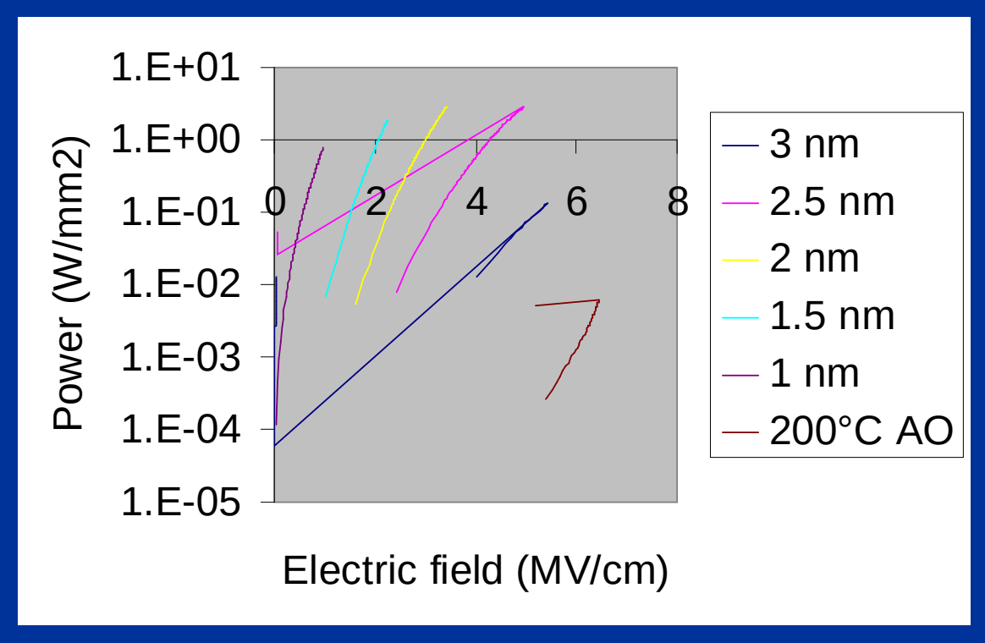




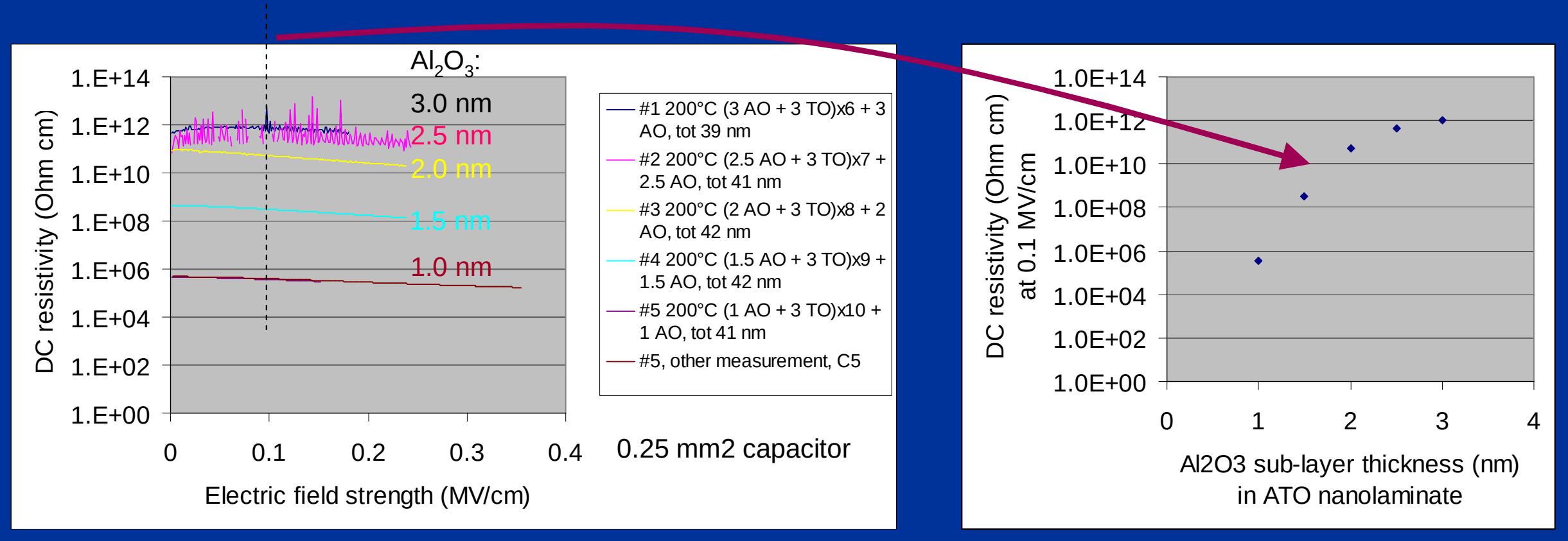
ELECTRICAL CHARACTERISTICS: ATO

ATO nanolaminates have leakage currents orders of magnitude higher than Al_2O_3. For Al_2O_3 sublayers ~2 nm and less, ATO nanolaminates withstand high-power stressing (> 1 W/mm^2) without catastrophic breakdown.

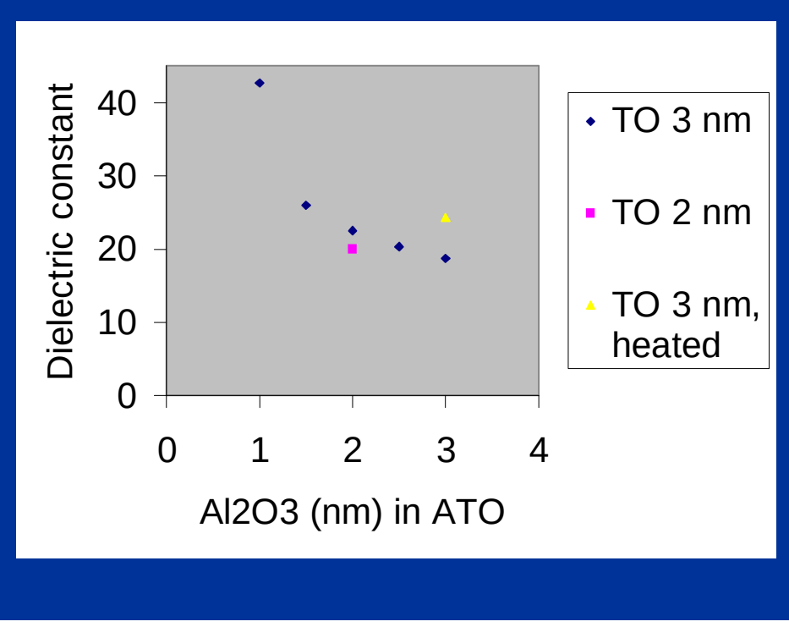


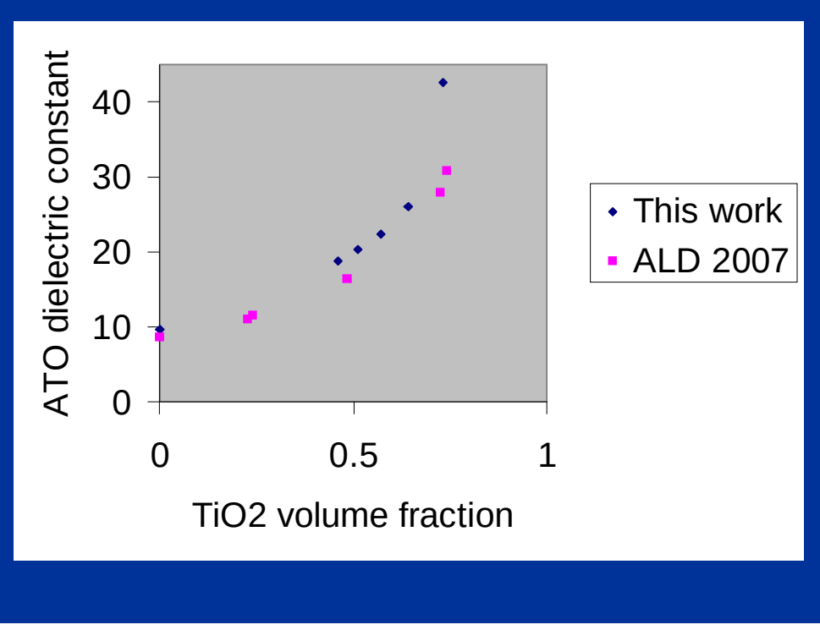


ATO resistivity can be accurately tuned:



ATO dielectric constant increases with TiO_2 content, together with leakage current





Note: Values of dielectric constant above ~30 not reliable due to high leakage current

CHANGES INDUCED BY ANNEALING

Samples annealed directly after ALD (N_2, 500°C, 30 min)

1. Al_2O_3, deposited at 200°C
    - No change in capacitance density
    - No change in leakage current (measurement at 0-2 V)
2. ATO nanolaminate, deposited at 200°C (3 nm sub-layers)
    - Leakage current increased somewhat
    - Measured dielectric constant increased slightly
3. TiO_2, deposited at 200°C
    - Resistivity decreased but remained on the order 10^1 Ohm cm
    - Uniformity over wafer remained constant

CONCLUSION

- Electrical properties of ATO nanolaminates can be adjusted in a wide range. The resistivity can be accurately tuned at 10^5-10^{12} Ohm cm. With pure TiO_2, lower values are achievable but, at the same time, more difficult to control. Dielectric constant ~25 is easily achieved with ATO nanolaminates.
- ATO layers can potentially be exploited in many applications, where controlled leakage currents and/or high dielectric constant are needed, including (RF)MEMS. With these particular "thermal" Al_2O_3 and TiO_2 ALD processes the deposition conditions are also flexible: ATO nanolaminates can be grown at least 110-300°C on various substrates, including those sensitive to oxidation.

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